IN THE CLAIMS

Please amend the claims as follows:

1. (Withdrawn) A bipolar transistor comprising:

a first semiconductor layer;

a collector layer formed in an upper surface region of the first semiconductor layer and containing an impurity of a first conductive type;

two isolation layers formed of an insulating film so that the isolation layers are spaced apart from each other and the collector layer is located therebetween;

a second semiconductor layer grown on the first semiconductor layer and the isolation layers, having a different band gap from that of the first semiconductor layer and containing an impurity of a second conductive type;

a third semiconductor layer formed on the second semiconductor layer and having a different band gap from that of the second semiconductor layer;

an insulating film formed on the third semiconductor layer and including an emitter opening portion; and

an emitter electrode formed of a polycrystalline semiconductor containing an impurity of the first conductive type so as to fill the emitter opening portion,

wherein a region of the third semiconductor layer which is in contact with the emitter electrode is an emitter layer containing an impurity of the first conductive type,

wherein a region of the second semiconductor layer interposed between the emitter layer and the collector layer is an intrinsic base layer containing an impurity of the second conductive type,

wherein regions of the second and third semiconductor layers each surrounding the intrinsic base layer together form an external base layer containing an impurity of the second conductive type,

wherein the external base layer is provided so as to extend between the isolation layers and has a silicide layer in a surface portion, and

wherein the emitter electrode has a thickness with which ions of the second-conductive-type impurity implanted into the emitter electrode to form the external base layer are diffused so that the concentration of the impurity is a low level in a lower portion of the emitter electrode.

2. (Withdrawn) The bipolar transistor of claim 1, wherein the thickness of the emitter electrode is in a range between not less than 200 nm and not more than 500 nm.

3. (Withdrawn) The bipolar transistor of claim 1, wherein a recess formed in aprt of an upper surface of the emitter electrode located over the emitter opening portion has an aspect ratio of 1/5 or less.

4. (Withdrawn) The bipolar transistor of claim 1, wherein ions of the second-conductive-type impurity are implanted into a region of the external base layer extending from a position of the substrate on a side of and under the emitter electrode to a distance of 230 nm from a boundary portion of the substrate between the emitter layer and the intrinsic base layer.

5. (Withdrawn) The bipolar transistor of claim 1, further comprising: an interlevel insulating film covering the emitter electrode and the external base layer; and a conductor plug formed so as to pass through the interlevel insulating film and being in contact with each of the isolation layers of the external base layer.

6. (Withdrawn) The bipolar transistor of claim 1, wherein the first semiconductor layer has a Si single crystal composition, and wherein the second semiconductor layer has a SiGe or

SiGeC mixed crystal composition.

7. (Currently Amended) A method for fabricating a bipolar transistor, comprising the steps of:

a) epitaxially growing on a first semiconductor layer of a first conductive type surrounded by isolation layers, a second semiconductor layer having a different band gap from that of the first semiconductor layer and containing an impurity of a second conductivity type so as to extend between the isolation layers;

b) epitaxially growing on the second semiconductor layer, a third semiconductor layer having a different band gap from that of the second semiconductor layer;

c) forming on the third semiconductor layer, an insulating film having an emitter opening portion;

d) forming on the third semiconductor layer and the insulating film, a polysilicon layer containing an impurity of the first conductivity;

e) patterning the polycrystalline layer and the insulating film [[layer]] to form an emitter electrode; and

f) implanting ions of an impurity of the second conductive type into the second and third semiconductor layers from a direction tilted from a perpendicular direction with respect to a surface of a substrate using the emitter electrode and the insulating film as masks,

wherein in the step c), the insulating film is in contact with the upper surface of the third semiconductor layer.

8. (Currently amended) The method of claim 7, further comprising the step of g) drive-in-diffusing an impurity of the first conductive type from the emitter electrode into the third

semiconductor layer to form an emitter layer in a region of the third semiconductor layer located under the emitter opening portion,

wherein in the step f), ion implantation of an impurity of the second conductive type is performed four times, with the substrate rotating by 90 degrees at a time ~~under the condition in which the second conductive type impurity does not go over a point of 230 nm from the boundary between the emitter layer and the second semiconductor layer to reach a portion of the substrate located closer to the emitter layer~~.

9. (Original) The method of claim 7, further comprising: after the step f),

the step h) of forming an insulator sidewall on side surfaces of the emitter electrode and the insulating film; and

the step i) of siliciding upper portions of the third semiconductor layer and the emitter electrode using the insulator sidewall as a mask.

10. (Currently amended) The method of claim 14 ~~7~~, wherein in the step d), ~~a~~ the second polycrystalline semiconductor layer has ~~having~~ a thickness of not less than 300 ~~200~~ nm and not more than 500 nm.

11. (Original) The method of claim 7,

wherein the first semiconductor layer has a Si single composition, and

wherein in the step a), the second semiconductor layer having a SiGe or SiGeC mixed crystal composition is grown.

12. (New) The method of claim 7, wherein in the steps a) and b), a film thickness of the second and third semiconductor layers, which are polycrystalline and serve as an external base layer over the isolation layers, is made thinner than a thickness of the second and third

semiconductor layers, which are polycrystalline and serve as an intrinsic base layer over the first semiconductor layer, by using UHV-CVD.

13. (New) The method of claim 7, wherein in the step f), a thickness of the emitter electrode is such that a concentration of the impurity of the second conductivity type, the impurity being implanted into the emitter electrode, is low under the emitter electrode.

14. (New) The method of claim 7, wherein the emitter electrode consists of a first polycrystalline semiconductor film and a second polycrystalline semiconductor film, and the polycrystalline layer is the second polycrystalline semiconductor film,

wherein the step c) includes the steps of:

c1) successively depositing on the third semiconductor layer, the insulating film and the first polycrystalline semiconductor film containing an impurity of a first conductivity type in this order;

c2) forming the emitter opening portion by patterning the first polycrystalline semiconductor film; and

c3) removing the insulating film inside the emitter opening portion, and

wherein in the step d), the second polycrystalline semiconductor film containing an impurity of a first conductivity type is formed on the third semiconductor layer and the first polycrystalline semiconductor film.